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Device Temperature and Heat Generation in Power Metal-Oxide Semiconductor Field Effect Transistors

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A numerical thermal–electrical model has been established for a typical power metal-oxide semiconductor field effect transistor (MOSFET) device in this work. The temperature and heat-generation distributions within the device are obtained and their effects on the device $I-V$ characteristics are examined. Drain currents in both the cutoff state and the on-state increase with an increase of ambient temperatures in the entire range of V_{ds} from the ohmic region to the breakdown region. The thermal impact on the $I_d - V_{ds}$ curves in the cutoff state and the on-state is displayed in terms of different prebreakdown behaviors. An abrupt temperature rise occurring before the traditionally known onset of the avalanche breakdown of the drain-body $p-n$ junction is observed in this work. Unlike the well-recognized avalanche breakdown mechanism, the microscopic mechanism for this temperature rise is not yet clearly understood. It is observed that, although the highest temperature does not occur in the channel region, the temperature gradient along the channel is the highest in the device domain. It is shown that the maximum heat generation occurs in the channel region. The magnitude of the heat generation in the channel region is found to be two orders higher than that in the drift region. This high local heat generation must be considered in the optimal design of power MOSFET devices to reduce the temperature, and more importantly, the temperature variation in the channel region for a more reliable performance of MOSFET in high-temperature applications.

Nomenclature

$D_{n,p}$ = diffusion coefficient
$D^T_{n,p}$ = thermal diffusion coefficient
E_g = effective bandgap energy
G = carrier generation rate
H = total heat-generation rate
I = current
$\boldsymbol{J}$ = vector of current density
$m^*_{n,p}$ = effective mass
N_a = acceptor concentration
N_d = donor concentration
n = electron concentration
P_p = thermoelectric power
p = hole concentration
q = charge of electron
R = carrier recombination rate
T = temperature
V = voltage
x = coordinate
y = coordinate
ε = absolute permittivity
κ = thermal conductivity
μ = mobility
$\phi_{n,p}$ = quasi-Fermi potential
ψ = electrostatic potential

Subscripts
d = drain
g = gate
n = electron
p = hole
s = source

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Introduction

METAL-OXIDE semiconductor field effect transistors (MOSFETs) have become widely used in the power electronic applications since their appearance in the 1980s, as a result of their improved on-state resistance, good off-state blocking voltage, and most importantly, much higher switching speed compared with that of bipolar junction power transistors (BJTs), which was the major type of power device that existed prior to the introduction of MOSFETs.

Because of its important and widespread applications, numerous academic and industrial research works[1] have been dedicated to the study of power MOSFET devices. Although newer devices such as insulated gate bipolar transistors (IGBTs), which are based on the combination of MOSFETs and bipolar junction transistors (BJTs), have also been widely used in current power applications, particularly in inverters, motor drives, and uninterrupted power supply (UPS), a better knowledge of MOSFETs remains valuable for the understanding of IGBTs because the latter devices operate on a very similar physical mechanism of MOSFETs.

Among previous works on power MOSFETs are the thermal–electrical studies addressing the problem of thermal impacts existing in the devices. These thermal–electrical studies have demonstrated that the self-heating effects have a substantial influence on the electrical characteristics of MOSFETs, as well as on the devices' performance in power electronic circuits. In recent years, the importance of thermal–electrical studies has been increasingly emphasized to accommodate the growing demand for power electronics devices to operate reliably in an ever-expanding range of thermal environments. Current and future thermal environments include high-temperature conditions such as applications in jet-engine sensors, geothermal measurements, nuclear-plant control instrumentation and automobile electronics, as well as some large temperature-varying conditions such as outer-space power supplies and aeronautical electronics.

Dikmen et al.[2] and Hsu and Chiu[3] studied the temperature dependence of MOSFET degradation caused by hot-electron injection in the temperature range of 0–100°C. They found that the reduced degradation at higher temperature is mainly caused by the decreased channel electric field compared with that of room temperature. Chen et al.[4] studied the temperature effects on MOSFET's driving capability and current/voltage gains. They observed that the temperature effects on the current gain are more sensitive at a temperature higher than room temperature, and that voltage gain and output resistance drop significantly at low temperatures. Singh and Baliga[5] measured the power MOSFETs at a temperature range between 77 and 300 K with a wide range of breakdown voltages. They found that as the temperature decreases, the breakdown voltage and on-state resistance decrease, whereas threshold voltage and transconductance increase. Zhu et al.[6] modeled the nonuniform heat dissipation in power transistors leading to the thermal runaway. Their results clearly indicated the existence of hot spots in the base-emitter contact region within BJTs.

As a further investigation of thermal phenomena in MOSFET devices, a two-dimensional numerical thermal–electrical model has been established for typical power MOSFET devices in this work. The temperature distribution and thermal–electrical interaction reflected by the variation of electrical characteristics with temperature are carefully examined in the model.

It should be pointed out that among the previously discussed thermal–electrical studies, very few results have been reported on the heat-generation rate and its role in the thermal–electrical interaction occurring in a wide range of temperatures. With the lack of precise knowledge about the distribution of the heat-generation rate within power semiconductor chips in the microscopic scale, many previous thermal modeling works have treated the heat-generation term simply as an evenly distributed heat source, which is far different from the actual heat-generation distribution, which has a highly concentrated zone within the channel region of MOSFET devices, as will be described later in this work. Therefore, another focus of this work, in addition to the issue of temperature effects on the electrical characteristics, is to identify the precise distribution of heat-generation rate within the MOSFET devices and to identify the effects of this heating distribution on the internal temperature field within the MOSFET devices.

Equations and Physical Models

The governing equations underlying the steady-state thermal–electrical interaction for solid-state semiconductor devices under consideration are

$$\nabla\cdot(\varepsilon\nabla\psi) + q(N_d - N_a + p - n) = 0 \tag{1}$$

$$-(1/q)\nabla\cdot\boldsymbol{J}_p + (G - R) = 0 \tag{2}$$

$$(1/q)\nabla\cdot\boldsymbol{J}_n + (G - R) = 0 \tag{3}$$

$$\nabla\cdot(k\nabla T) + H = 0 \tag{4}$$

Equations (1–4) represent the Poisson equation, electron continuity, hole continuity, and energy conservation, respectively. The unknown electrical state-variables in Eqs. (1–3) are ψ, n, and p, respectively, denoting the electrostatic potential, electron concentration, and hole concentration, respectively. The unknown thermal state-variable T, in Eq. (4), denotes the lattice temperature of the semiconductors. The material parameters in Eqs. (1–4) are ε, q, and κ of the semiconductor material. H will be modeled later in this work. The variables $\boldsymbol{J}_n$ and $\boldsymbol{J}_p$ denote electron and hole current density vectors along the direction of the electric currents. The current densities of electrons and holes, in turn, can be expressed as

$$\boldsymbol{J}_n = -q\mu_n n\nabla\psi + qD_n\nabla n + qnD_n^T\nabla T \tag{5}$$

$$\boldsymbol{J}_p = -q\mu_p p\nabla\psi - qD_p\nabla p - qpD_p^T\nabla T \tag{6}$$

where μ_n and μ_p are the electron and hole mobilities, respectively; D_n^T and D_p^T are the thermal diffusion coefficients for electrons and holes, respectively; and D_n and D_p denote the corresponding diffusion coefficients.

The physical models of the preceding parameters used in this work fully incorporate temperature effects. Taking the temperature-dependent intrinsic lattice scattering into consideration, the carrier mobilities, μ_n and μ_p, are modeled by empirical models based on empirical data for silicon[7]:

$$\mu_n = 55.24 + \frac{1425(T/300)^{-2.3} - 55.24}{1 + (T/300)^{-3.8}[N_{\text{total}}/(1.072\times 10^{17})]^{0.73}} \tag{7}$$

$$\mu_p = 49.74 + \frac{479.4(T/300)^{-2.2} - 49.74}{1 + (T/300)^{-3.7}[N_{\text{total}}/(1.606\times 10^{17})]^{0.70}} \tag{8}$$

where N_{total} is the sum of the donor and acceptor doping concentrations in cm^{-3}, $N_{\text{total}} = N_a + N_d$; and T is the lattice temperature in Kelvin.

The diffusion coefficients D_n and D_p are usually expressed in terms of the carrier mobilities using Einstein relations as

$$D_n = (kT/q)\mu_n \tag{9}$$

$$D_p = (kT/q)\mu_p \tag{10}$$

where k is the Boltzmann constant. Similarly, the thermal diffusion coefficients D_n^T and D_p^T are expressed as

$$D_n^T = (r_n - \tfrac{3}{2})\mu_n(k/q) \tag{11}$$

$$D_p^T = (r_p - \tfrac{3}{2})\mu_p(k/q) \tag{12}$$

where r_n and r_p are numerically adjusted coefficients, depending on the type of application. For power MOSFET devices, the representative value for both r_n and r_p is $\frac{5}{2}$. A temperature-dependent model is used in this work for the silicon thermal conductivity, namely, κ, which is given as

$$\kappa(T) = 1.54(T/300)^{-4/3} \tag{13}$$

For computational convenience, n and p in Eqs. (2) and (3) are usually substituted by the corresponding quasi-Fermi potentials, ϕ_n and ϕ_p, which have the same order of magnitude as the electrostatic potential ψ, in governing Eqs. (1–3). The quantities ϕ_n and ϕ_p are defined as

$$\phi_n = \psi - (kT/q)\ell n(n/n_{ie,n}) \tag{14}$$

$$\phi_p = \psi + (kT/q)\ell n(p/n_{ie,p}) \tag{15}$$

where $n_{ie,n}$ and $n_{ie,p}$ are the effective intrinsic concentrations for electrons and holes, respectively, which, in turn, can be expressed as

$$n_{ie,n} = 2\gamma_n(2\pi kT/h^2)^{3/2}(m_n^* m_p^*)^{3/4}\exp[-(E_g/2kT)] \tag{16}$$

$$n_{ie,p} = 2\gamma_p(2\pi kT/h^2)^{3/2}(m_n^* m_p^*)^{3/4}\exp[-(E_g/2kT)] \tag{17}$$

where h represents Planck's constant; m_n^* and m_p^* represent the effective masses for the conduction and valence bands, respectively; and γ_n and γ_p represent the degeneracy factors for electrons and holes, respectively, reflecting the deviation of Boltzmann statistic approximations from Fermi–Dirac statistics.

With respect to the physical models for the carrier recombination terms in Eqs. (2) and (3), two recombination processes that are of utmost importance in MOS-type devices,

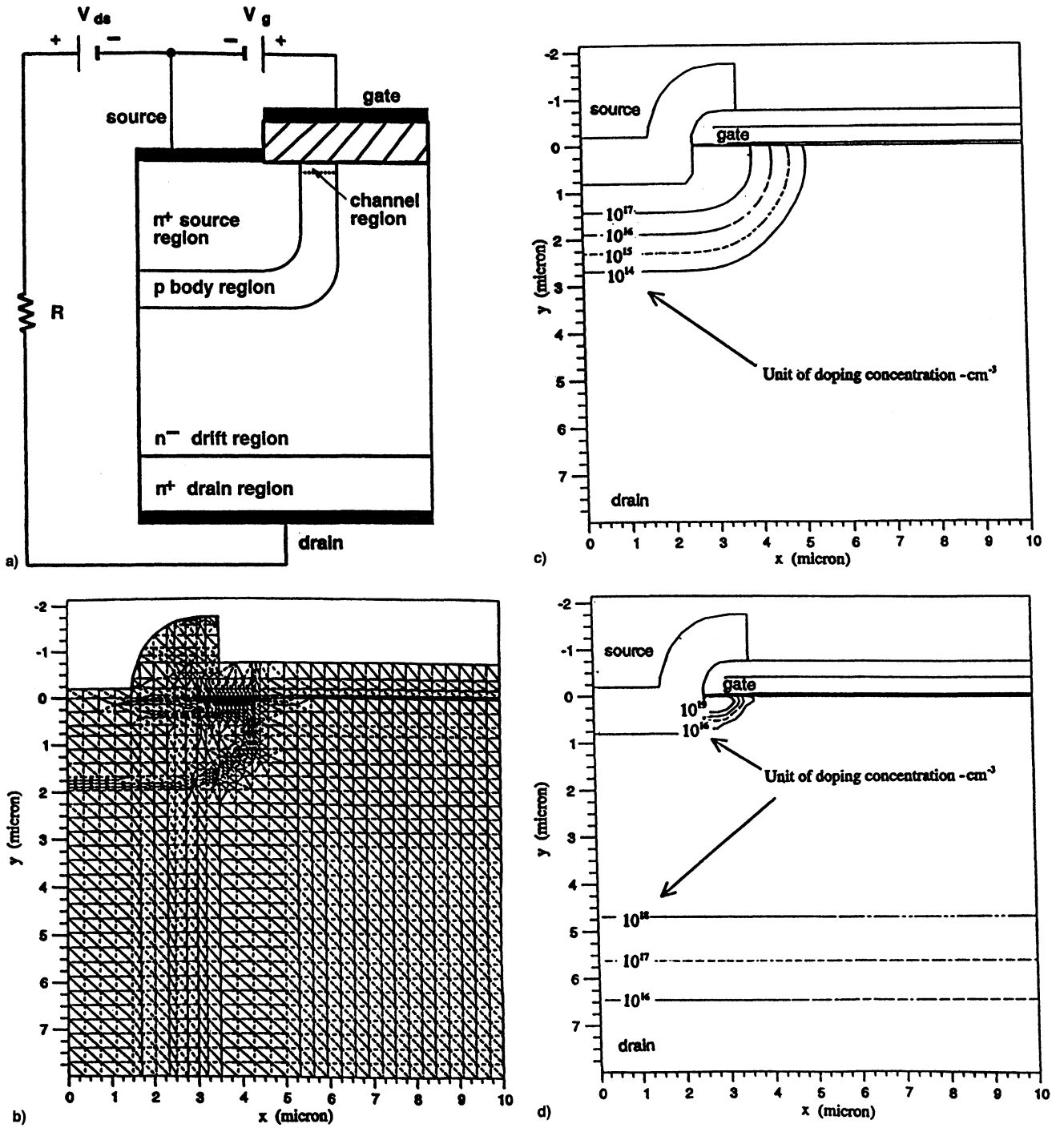

Fig. 1 a) Diagram for the MOSFET circuit, b) mesh for the numerical model of the MOSFET, c) acceptor doping profile in the MOSFET, and d) donor doping profile in the MOSFET.

namely, the Shockley–Read–Hall (SRH) and Auger recombination, are included as

$$R = R_{\text{Aug}} + R_{\text{SRH}} \tag{18}$$

where R_{Aug} and R_{SRH} represent the Auger and SRH recombination rates, respectively, which, in turn, are expressed as

$$R_{\text{Aug}} = 8.3 \times 10^{-32}(pn^2 - nn_{ie,n}^2) + 1.8 \times 10^{-31}(np^2 - pn_{ie,p}^2) \tag{19}$$

$$R_{\text{SRH}} = \frac{(pn - n_{ie,n}n_{ie,p})}{\tau_n(p + n_{ie,p}) + \tau_p(n + n_{ie,n})} \tag{20}$$

where τ_n and τ_p are carrier lifetimes for electron and holes, respectively. The numbers in Eq. (19) are obtained from empirical data for silicon.[7]

For the physical models of the carrier generation terms in Eqs. (2) and (3), the generation of electron-hole pairs during the Selberherr process of impact ionization that is dominant in high-temperature devices is taken into consideration. This is expressed as

$$G = \alpha_n(|J_n|/q) + \alpha_p(|J_p|/q) \tag{21}$$

where α_n and α_p are the temperature-dependent electron and hole ionization rates, respectively.

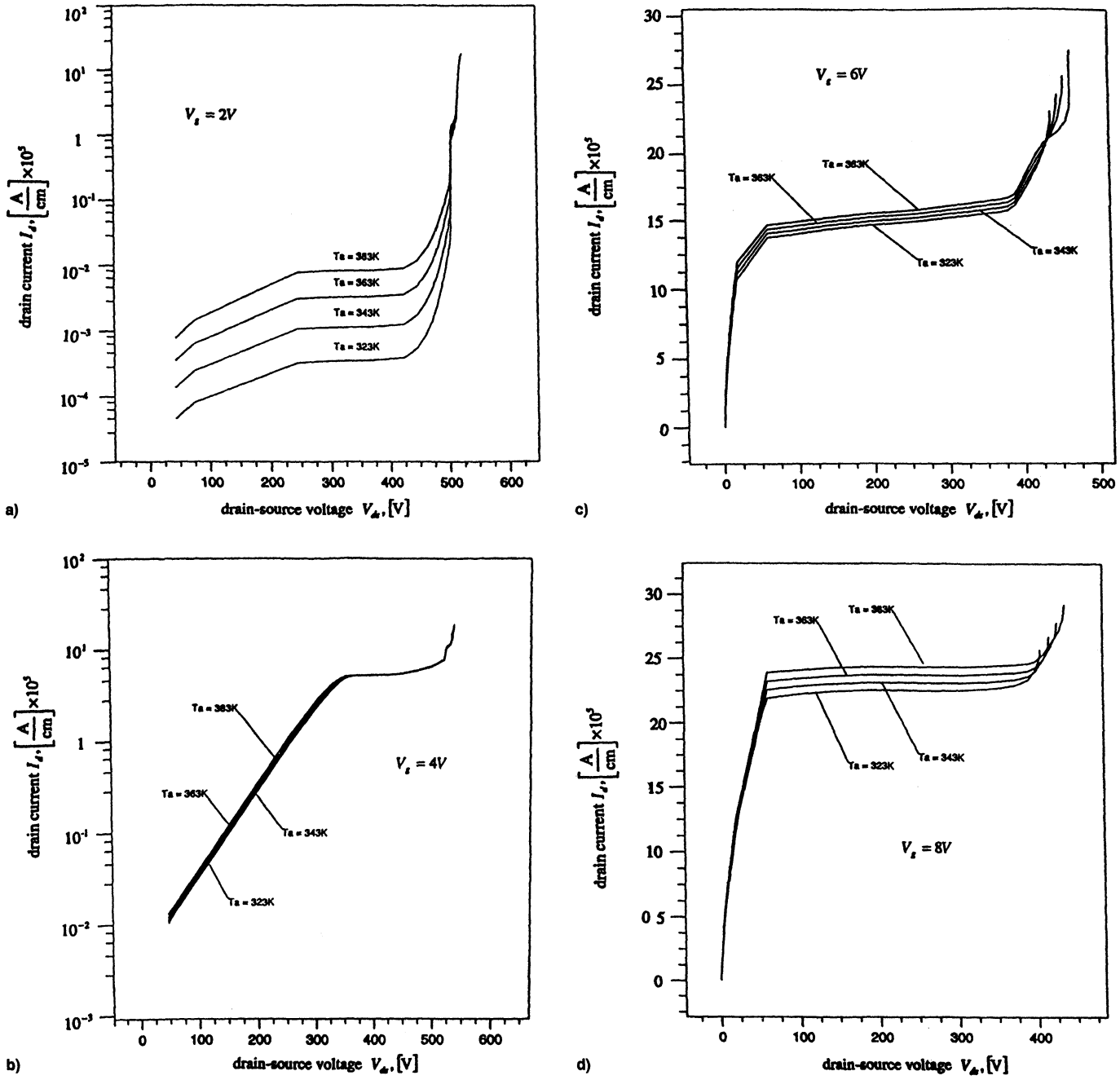

Fig. 2 Current–voltage characteristics for different ambient temperatures and gate biasings. V_g = a) 2, b) 4, c) 6, and d) 8 V.

The heat-generation term H in Eq. (4) has a crucial importance in the thermal–electrical computations for power semiconductor devices. In this work, it is modeled as

$$H = H_{\text{Joule}} + H_{\text{recom}} + H_{\text{PT}} \tag{22}$$

which is based on a rigorous thermodynamics analysis of Wachutka,[8] where the three terms on the right-hand side of Eq. (22), H_{Joule}, H_{recom}, and H_{PT}, represent the traditional Joule heat, the recombination heat, and the Peltier–Thomson heat, respectively. H_{Joule} can be modeled as

$$H_{\text{Joule}} = (\boldsymbol{J}_n + \boldsymbol{J}_p)\cdot\boldsymbol{E} \tag{23}$$

where $\boldsymbol{E}$ is the electric field vector. H_{recom} generated from the carrier recombination process is modeled as

$$H_{\text{recom}} = qR\lfloor\phi_p - \phi_n + T(P_p - P_n)\rfloor \tag{24}$$

where P_p and P_n are the thermoelectric power for electrons and holes, respectively, which are given as

$$P_n = -(k/q)[S_n + \tfrac{5}{2} - \ell n(n/N_c)] \tag{25}$$

$$P_p = -(k/q)[S_p + \tfrac{5}{2} - \ell n(p/N_v)] \tag{26}$$

where parameters S_n and S_p depend on the electron–lattice scattering mechanism and are both set to the typical value of $+\frac{3}{2}$ in this work for the ionized impurity scattering in the MOSFET channel region. H_{PT}, in the heat-generation expression of Eq. (22), is modeled as

$$H_{\text{PT}} = -T(\boldsymbol{J}_n\cdot\nabla P_n + \boldsymbol{J}_p\cdot\nabla P_p) \tag{27}$$

It should be noted that H_{PT} is small compared with the other two heat-generation terms, H_{Joule} and H_{recom}; however, it can have a substantial contribution on the total heat generation

when a large temperature gradient exists in the semiconductor devices.

Equations (1–4) are discretized and solved by the Newton projection scheme in the time domain. In this scheme, the equations are fully coupled with the temperature-dependent model Eqs. (5–26). At each time step, convergence is considered to be obtained when the changes of all variables between two consecutive iterations are within 0.1%.

Results and Discussion

A schematic of a typical power MOSFET structure studied in this work with the external circuit in which the device is embedded is shown in Fig. 1a. The source terminal is electrically grounded. The gate terminal is connected to the source terminal through a controlling voltage source V_g, and the drain terminal is connected to the source terminal through a voltage source V_{ds} and an external resistor R. The polarities of both the gate voltage V_g and the drain-source voltage V_{ds} are shown in Fig. 1a. During the simulation, the gate and drain terminals are biased to varying values of V_g and V_{ds}, and the values of the current flowing through the drain terminal I_d are extracted for the gate and drain biasing.

Figure 1a also shows the $n^+pn^-n^+$ structure of the enhancement-mode n-channel MOSFET. Typical doping concentrations are assigned to the structure. The heavy doping of donor (phosphorous) concentration in the source region is 1.6×10^{19} cm^{-3}, and the heavy doping of the acceptor (arsenic) concentration in the drain region is 2.1×10^{19} cm^{-3}. The drift layer is lightly doped at 2.3×10^{14} cm^{-3} to sustain a large applied voltage when the MOSFET is in the blocking state. The p-type body layer is doped at 10^{16} cm^{-3}. The thickness of the gate-oxide layer is 100 Å. The mesh distribution used in the discussion of Eqs. (1–4) is shown in Fig. 1b. To obtain a large enough resolution in the channel region to precisely capture the abrupt variation of the electric field and the current densities, a large number of nodes is assigned to the small channel region with dimensions of 0.41 μm in thickness and 1.0 μm in width. When the numbers of nodes in x and y direction are doubled, the variation of the maximum heat generation obtained is less than 1%, indicating sufficient numerical accuracy. The acceptor doping profile in the MOSFET structure is shown in Fig. 1c, and the donor doping profile is shown in Fig. 1d.

For the thermal boundary condition, the drain side and the source section on the top side of the MOSFET structure are applied with a constant ambient temperature condition, $T = T_a$. The gate section of the top side is assumed to be thermally isolated. The two vertical boundaries of the MOSFET cell structure are assumed to be adiabatic, considering the symmetry of the structure. This thermal boundary setting corresponds to the usual source-up packaging configuration, in which a powerful heat sink is mounted onto the substrate, which, in turn, is mounted to the drain side of the semiconductor wafer. The amount of heat that is dissipated through the paths other than the heat sink is generally negligibly small compared with that through the heat sink, a fact justifying the previous adiabatic boundary condition assumption at the gate section on the top side of the structure.

The temperature-dependent forward-characteristic curves of I_d and V_{ds}, for different V_g, are plotted in Figs. 2 and 3. Figures 2a and 2b correspond to $V_g = 2$ and 4 V, respectively, in which case the MOSFET is in the cutoff state as V_g is less than the threshold $V_{GS(th)}$ necessary to turn on the MOSFET. Figures 2c and 2d show the forward characteristic curves for $V_g = 6$ V and $V_g = 8$ V, respectively, at the full computation range of V_{ds} from 0.001 V to the breakdown voltage. To clearly demonstrate the details of the breakdown sections of the I–V curves in Figs. 2c and 2d, enlarged plots for these breakdown sections are provided in Figs. 3a and 3b for $V_g = 6$ and 8 V, respectively. In each figure, the four curves correspond to different ambient temperatures T_a at 323, 343, 363, and 383 K.

In Figs. 2a and 2b, which correspond to the cutoff state, the drain current increases with the ambient temperature in the entire range of V_{ds} from the ohmic region to the breakdown region. This increase of the drain current can be explained by the following fact. Because V_g at the cutoff state is not large enough for the p-type body region beneath the gate-oxide layer to be inverted to n type, the channel region cannot be established. The drain current at the cutoff state is basically generated by the intrinsic lattice scattering, which will be intensified by a higher lattice temperature. It can also be noted that the different ambient temperatures do not have a significant impact on the breakdown voltage for the MOSFET at the cutoff state. It is shown in Figs. 2a and 2b that, in the V_{ds} range prior to the breakdown point, the drain current starts to increase rapidly at about the same V_{ds} for the four curves corresponding to the four ambient temperatures. The derivative of I_d with respect to V_{ds} is found to decrease with an increase in the ambient temperature.

Figures 2c and 2d correspond to the device at the on-state. Similar to that of the cutoff state, the drain current increases

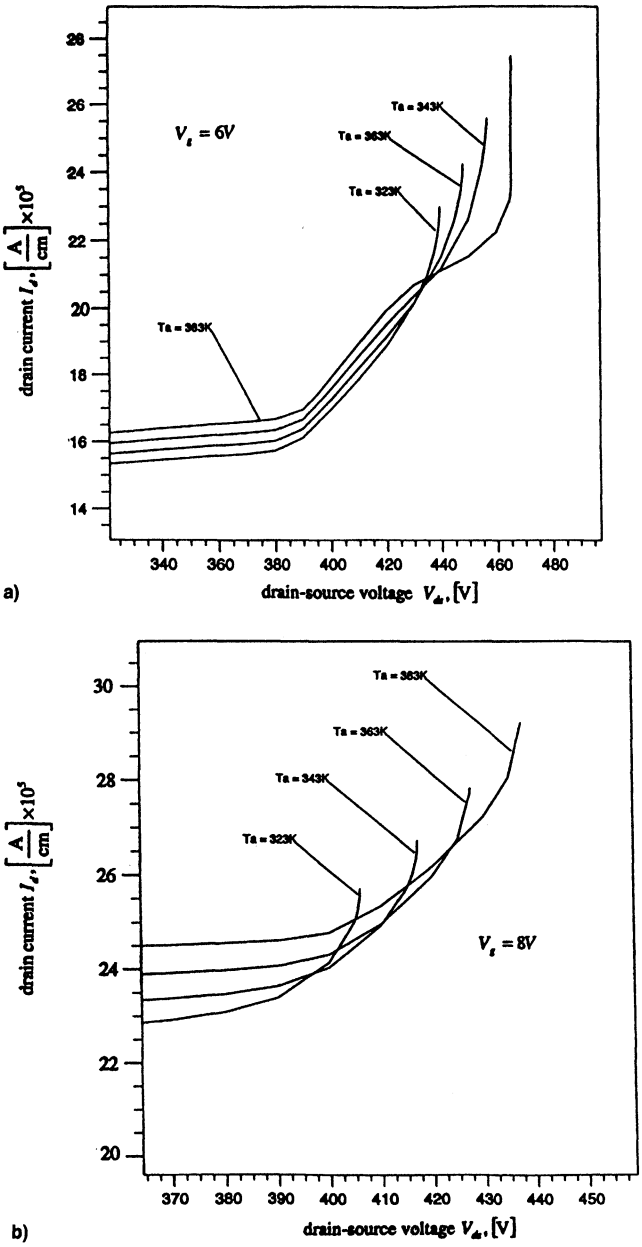

Fig. 3 Breakdown section of current–voltage characteristics for different ambient temperatures and gate biasings. V_g = a) 6 and b) 8 V.

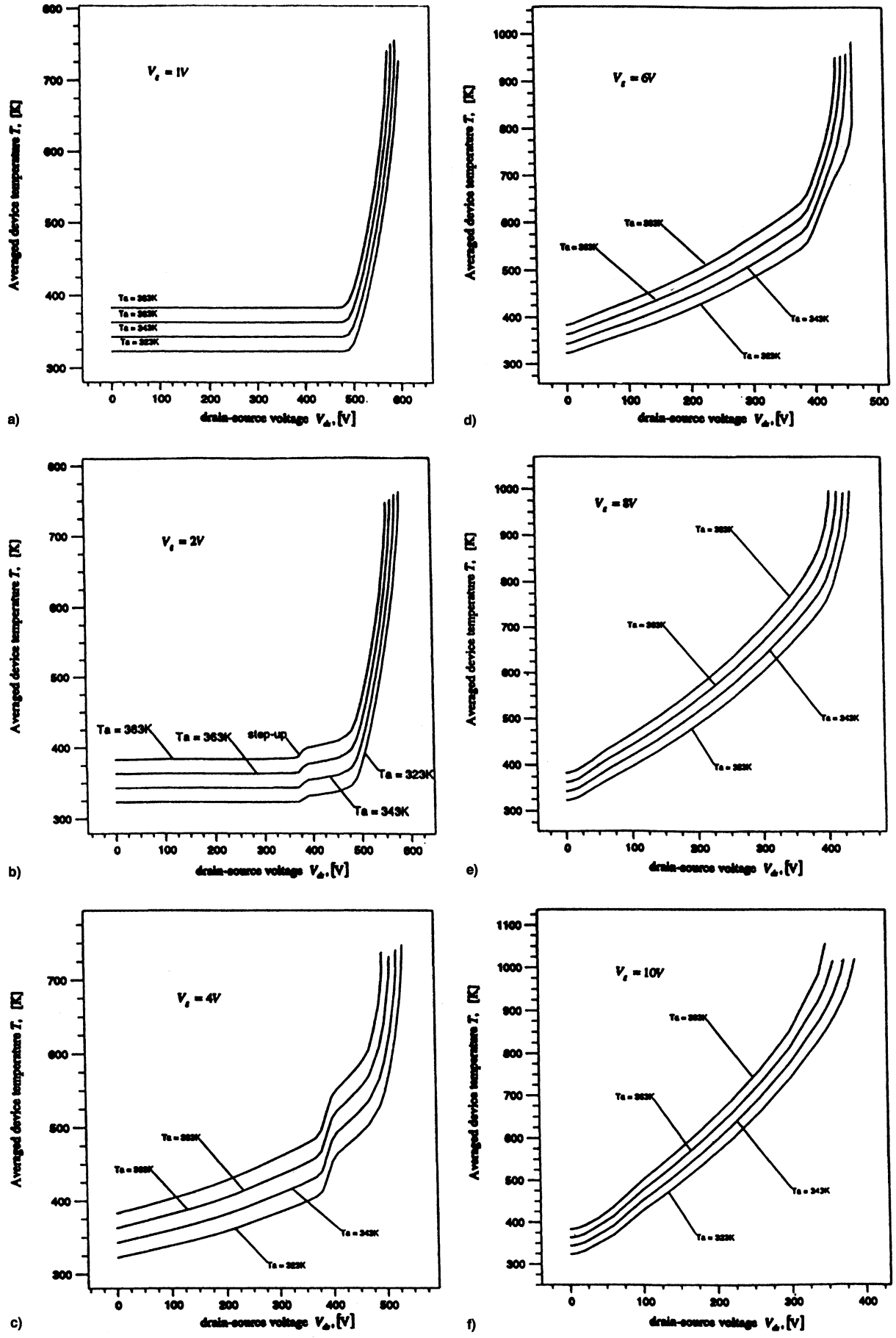

Fig. 4 Averaged device temperature at different ambient temperatures and gate biasings. V_g = a) 1, b) 2, c) 4, d) 6, e) 8, and f) 10 V.

with the ambient temperature, but to a lesser degree compared with the cases for the cutoff state. The temperature influence on the $I_d - V_{ds}$ curves in the cutoff state and the on-state can be seen in the prebreakdown behavior shown in Figs. 2c and 2d for $V_g = 6$ and 8 V, respectively. For the on-state case, the drain current in low-temperature cases starts to rise before it does for the high-temperature cases, indicating an earlier occurrence of major avalanche breakdown for lower device temperature. It can also be seen in Figs. 3a and 3b that the drain current for a higher temperature case increases at a slower rate against V_{ds} until it approaches the breakdown point, where the rate increases significantly.

Figure 4 illustrates the average device temperature in the MOSFET structures as it varies with V_{ds} for different ambient temperatures and gate voltages. Figures 4a–4f correspond to V_g = 1, 2, 4, 6, 8, and 10 V. It can be seen in Fig. 4a that with the gate voltage lower than the threshold voltage in the cutoff state, the self-heating caused by the small leakage current is negligibly small, so that the device temperature remains at the ambient temperature. The self-heating in the on-state device, in contrast, is significant, even at the low end of the drain-source voltage calculated in this work, as shown in Figs. 4c–4f. As a result, the device temperature is increased by the self-heating effect at a steady rate before V_{ds} reaches the breakdown point. It is found that the temperature rise of the average device temperature over the ambient temperature is about the same at different ambient temperatures, and is increased only with gate voltages.

Another interesting phenomenon that has not, to the best of our knowledge, been reported by previous works, is an abrupt

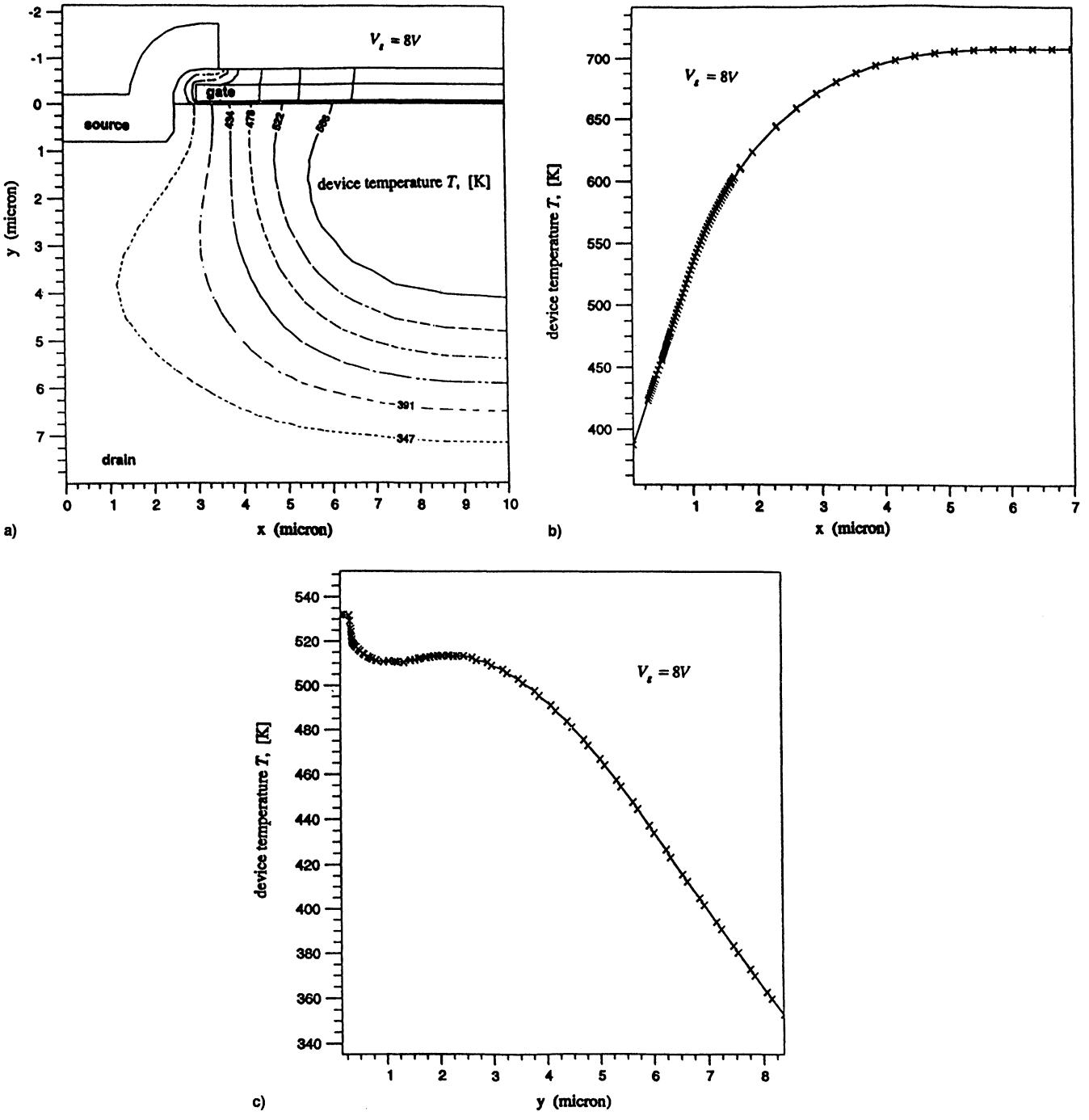

Fig. 5 Temperature distributions within the studied MOSFET device for V_g = 8 V: a) contour plot, b) distribution in the lateral direction (along the channel region), and c) distribution in the vertical direction.

temperature step-up occurring before the traditionally known onset of the avalanche breakdown of the drain-body $p-n$ junction. This temperature step-up is initially seen in Fig. 4b, where the MOSFET is still in the cutoff state. The rate of device temperature rise with respect to V_{ds} increases abruptly within a very short range of V_{ds}, after which the rate slows down toward the value that is slightly larger than the original rate before the step-up region. With an increase in the gate voltage, the magnitude of the temperature rises during the step-up increase. The position of the drain voltage range moves toward higher voltage with an increase of V_g. The position shift is clearly shown in Figs. 4b–4f by the step-up, as distinguished from the final breakdown in Fig. 4b for V_g = 2 V, moving toward higher voltage in Figs. 4c and 4d for V_g = 4 and 6 V, and finally merging with the ultimate breakdown region in Figs. 4e and 4f for V_g = 8 and 10 V. Unlike the well-recognized avalanche breakdown mechanism, the microscopic mechanism for this temperature step-up observed in this work is not yet clearly understood. It appears that, as the drain-source voltage increases, a partial avalanche breakdown takes place in the MOSFET structure. Furthermore, the device appears to have the capability to recover itself from the partial avalanche breakdown, postponing the full development of the avalanche breakdown to a higher drain-source voltage. The mechanism of this temperature step-up phenomenon is believed to be worthy of further investigation, because a clearer understanding of this recovery capability of the device from partial breakdown can provide physical insight for protection against MOSFET breakdown.

Figure 5 shows the temperature distribution within the device at V_g = 8 V. The spatial temperature distribution patterns at different gate voltages are similar to each other. As can be seen, the highest temperature occurs at the upper-right region of the simulated device domain, corresponding to the drift

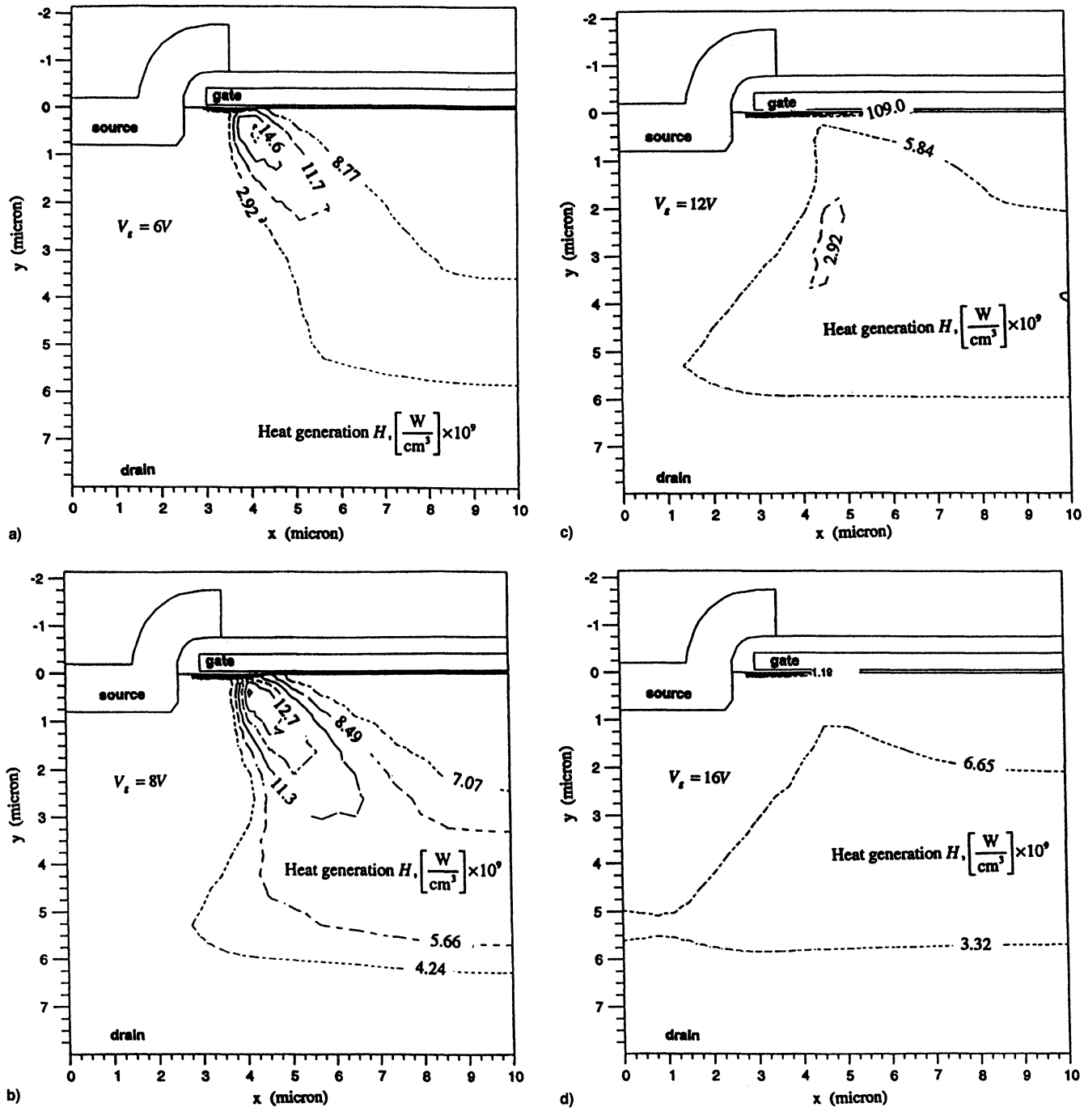

Fig. 6 Heat-generation distributions within the studied MOSFET device contour plot for V_g = a) 6, b) 8, c) 12, and d) 16 V.

region that is directly underneath the gate-oxide layer, which has a poor thermal conductivity. The position of the highest temperature is close to the centerline of the MOSFET cell structure. The temperature contour lines starting at the base side (right side) extend horizontally to the source side (left side), shifting upward in the body and drift region and ending up as vertical lines at the channel region.

The temperature distribution in the channel region is of particular importance to the device performance because this is where the inversion mechanism governing the operation of MOSFET takes place. Although the highest temperature does not occur in the channel region, as has been discussed earlier, the temperature gradient along the channel is the highest in the device domain. This is indicated by the large number of contour lines crowding in the channel region. This large temperature gradient is caused by the highly nonuniform distribution of heat generation concentrated in this region. It should be pointed out that this large temperature gradient in the channel region should be reduced in the power MOSFET design, because it may cause significant variation in electrical parameters such as carrier mobilities, and in particular, it may also generate a substantial amount of heat locally through the Peltier–Thomson heating mechanism, as modeled in Eq. (27).

Figure 5b shows the temperature along a horizontal line through the channel region, starting at the source metallization and ending at the right side, namely, the centerline of the MOSFET cell structure. Again the high-temperature gradient is clearly shown in the channel region. Figure 5c shows the temperature distribution on a vertical line starting from the upper edge of the gate oxide and ending at the bottom side of

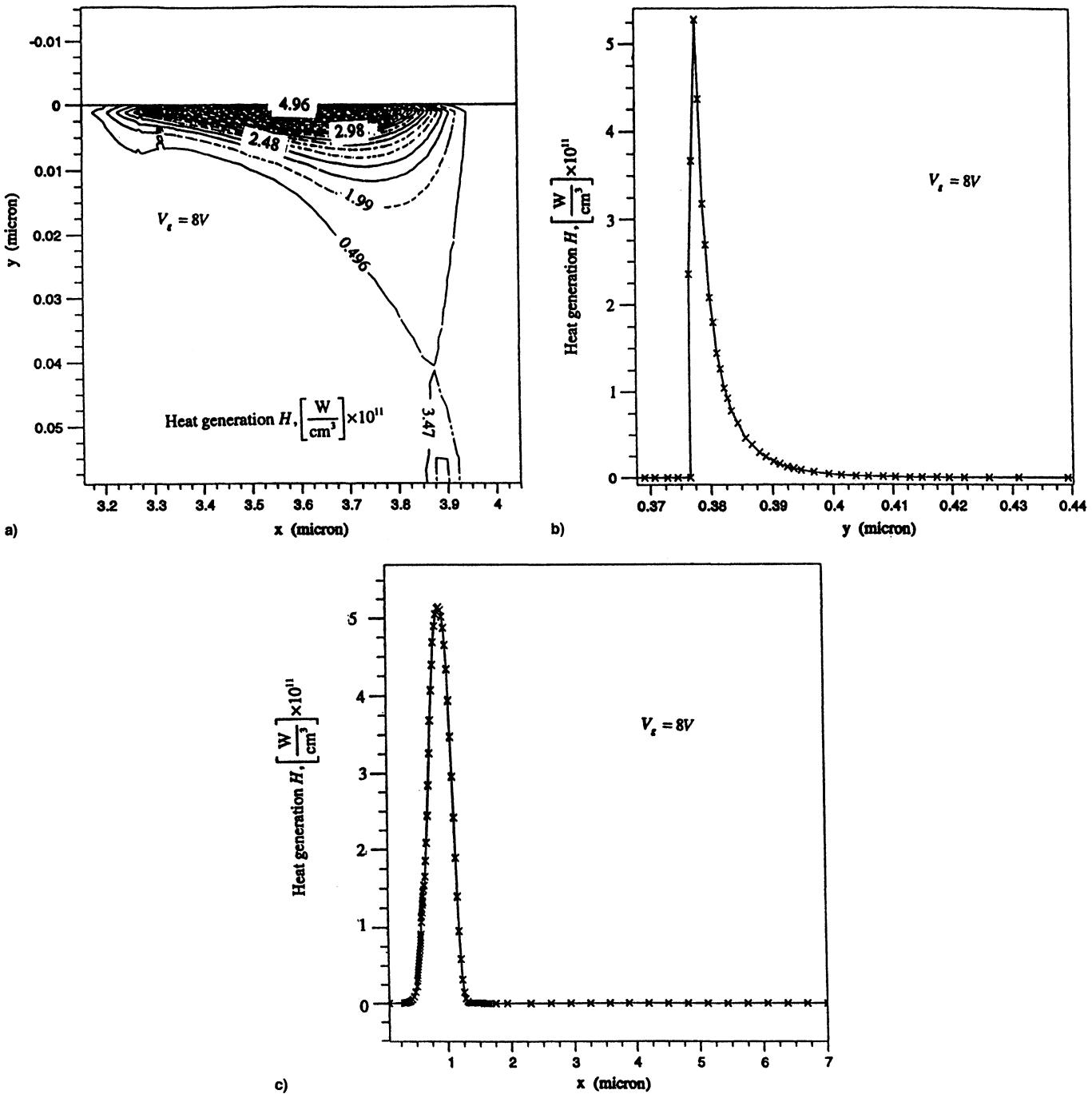

Fig. 7 Heat-generation distributions within the channel region for V_g = 8 V: a) enlarged contour plot in the channel region, b) distribution in the vertical direction, and c) distribution in the lateral direction (along the channel region).

the drain region. The temperature curve plotted in Fig. 5c shows a sharp decrease in the gate-oxide region. This sharp decrease is slowed down near the gate-metallization region, attaining a flat shape around the channel and body region, and finally, it decreases evenly through the body and drift region. This is a desirable feature for MOSFET operation.

The heat-generation distributions computed based on Eq. (22) are shown in Figs. 6 and 7. Figures 6a–6d show the heat-generation contour plots within the device at the different gate voltages corresponding to the on-state condition. The results for the cutoff state, however, are excluded from Fig. 6, because the heat generation is negligible and has no significant effect on device characteristics. It is found that for the different gate voltages the heat generation in the source and base regions is negligibly small compared with the heat generation in the drift and channel regions. It is also observed that the heat generation in the drift region is distributed quite evenly. The low doping profile in the drift region required to sustain a certain breakdown voltage produces a significant drift resistance, which translates to a significant amount of Joule heating when the drain current flows through the drift resistance. The total amount of heat generation within this drift region contributes to a major portion of the total heat generation of the MOSFET investigated in this work, as has been observed by Singh and Baliga.[5]

The maximum heat generation occurs in the channel region for all of the computation cases considered in this work, corresponding to different gate voltages ranging from 6 to 18 V. The magnitude of the heat generation in the channel region is two orders of magnitude higher than that in the drift region. The distribution is restricted within the inversion layer underneath the gate oxide. This high heat generation is caused by the product of the potential drop along the inversion layer and the extremely high current density in the same region. Figure 7a shows the detailed distribution in the channel region for V_g = 8 V. Distributions of the heat generation for other gate voltages are similar to Fig. 6e (with the magnitude increasing with V_g). The heat-generation distribution in the directions that are along and perpendicular to the inversion layer is plotted in Figs. 7b and 7c, respectively. It can be seen in Fig. 7b that the maximum magnitude of heat generation is located at approximately the center of the channel thickness vertically. This heat generation decreases rapidly to 10% of its peak value within a small distance of 0.002 μm from the location of the maximum value. This highly localized distribution also holds true in the direction along the channel, as indicated in Fig. 7c. The maximum heat generation is located at approximately the center of the channel width laterally. It decreases rapidly to 10% of its peak value within a 0.25-μm distance toward either the source or the gate end of the inversion layer.

The existence of the highly concentrated heat-generation distribution in the channel region as it is shown in Figs. 6 and 7, has not, to the best of the authors' knowledge, been reported in the literature. It must be pointed out that, although the total amount of heat generated within the small channel region is not comparable with the contribution from the drift region, the high local heat-generation concentration must be considered in the optimal design of power MOSFET devices for reducing the temperature variation in the channel region. This results in a more reliable MOSFET performance for high-temperature applications.

Conclusions

A two-dimensional numerical thermal-electrical model has been established for a typical power MOSFET device. The temperature and heat-generation distributions within the device are obtained and their effects on the device $I-V$ characteristics are examined. Drain currents in both the cutoff state and the on-state increase with an increase of ambient temperatures in the entire range of V_{ds}, from the ohmic region to the breakdown region. The temperature influence on the $I_d - V_{ds}$ curves in the cutoff and on-states is manifested in term of different pre-breakdown behaviors. An abrupt temperature step-up occurring before the traditionally known onset of the avalanche breakdown of the drain-body $p-n$ junction is observed in this work. Unlike the well-recognized avalanche breakdown mechanism, the microscopic mechanism for this temperature step-up is not yet clearly understood.

It is also observed in this work that although the highest temperature does not occur within the channel region, the temperature gradient along the channel is the highest in the device domain. It is shown that the maximum heat generation occurs within the channel region. The magnitude of the heat generation in the channel region is found to be two orders of magnitude higher than that in the drift region. The high local heat generation must be considered in the optimal design of power MOSFET devices to reduce the temperature, and more importantly, the temperature variation within the channel region for a more reliable MOSFET performance for high-temperature applications.

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